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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,734	12/22/2000	Colin Davidson	0325.00436	4619

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EXAMINER	
SUNDARAM, T R	
ART UNIT	PAPER NUMBER
2858	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/747,734	Colin Davidson et al.
Examiner	**Art Unit**
T. R. Sundaram	2858

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 16, 2002* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-23* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Oct 16, 2002* is/are a) ☐ accepted or b) ☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The proposed drawing corrections that have been submitted by the Applicants on October 16, 2002, in response to the objections in the First Office Action on Merits (FOAM, dated July 17, 2002, have been approved by the Examiner.

2. Figure 1 should also be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Figure 1 is discussed in the background section of the specification (page 1), and the correlation between T_{sd} and probability of failure is admitted as known in prior art. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The new abstract submitted by the Applicants on October 16, 2002 is approved by the Examiner.

Earlier Claim Rejections and Applicants' Response

4. In response to the rejection of claims 1-20 being rejected under 35 U.S.C. 103(a) as being unpatentable over *Ahmad et al.,* in view of *Gascoyne* and *Agarwal et al.*, in the FOAM, the

Applicants have amended some claims, submitted three new claims (claims 21-23) and have also submitted detailed arguments on the patentability of the amended claims.

The Examiner has considered the amendments and the Applicants' arguments in full, but finds them only partially persuasive. In particular, since the claims as presently recited are deemed not to be patentable over prior art, new rejections are given herein for claims 1-23. Some of the arguments of the Applicants are then addressed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by *Malek-Khosravi et al.*

Malek-Khosravi et al. discloses an integrated circuit (title; abstract; and column 1, line 9) comprising: means for generating a test signal (Fig. 1) having a predetermined pulse width (column 2, lines 59-66) in response to a control input (Fig. 1; and column 2, line 33); and means for predicting failure of part or all of said integrated circuit in response to said test signal (column 3, lines 17-28 and line 37).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-10 and 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Ahmad et al.*, in view of *Malek-Khosravi et al.*, and *Applicant's own admitted prior art.*

Regarding claim 1, *Ahmad et al.* discloses an integrated circuit (13, Fig. 1 and Fig. 2) comprising: a test circuit (upper half, Fig. 2; and column 3, lines 62-63) configured to generate a test signal (53 and 55, Fig. 2; and column 6, lines 14 ff) and can be used to predict failure of said integrated circuit (column 1, lines 16-17; column 2, lines 63-67; column 4, line 29).

Ahmad et al. does not expressly disclose a test signal having a predetermined pulse width in response to a control input, wherein said test signal tracks process corners and which can be used to predict failure of said integrated circuit. Albeit, *Ahmad et al.* discloses (Figs. 8-10) various methods for performing a self-test on the built-in circuits.

Malek-Khosravi et al. discloses an integrated circuit chip (abstract; Fig. 1) configured to generate a test signal with a predetermined pulse width (Fig. 2; and column 1, lines 9-24) in response to a control input (Fig. 1; and column 2, lines 31-34), and to determine the minimum

pulse width in order for the circuit to operate properly (column 1, lines 21-24) by tracking process corners (Fig. 2).

Applicant's own admitted prior art (Fig. 1; and pages 1-2 of specification) discloses that there is a definite correlation between write end time (minimum pulse width for proper operation of the cell) and probability of failure.

At the time of the invention, it would have been obvious for a person of ordinary skill in the art to have combined into *Ahmad et al.* the teachings of *Malek-Khosravi et al.*, in light of the *Applicant's own admitted prior art*, for the purpose of obtaining an integrated-circuit test circuit that can be used to predict failure of the integrated circuit, so that circuits with a high probability of failure can be eliminated from further testing and/or can be repaired.

Regarding claim 2, *Ahmad et al.* discloses that the control input (53, Fig. 2) comprises a write enable input (Fig. 8; and column 9, lines 26 ff).

Regarding claim 3, *Ahmad et al.* discloses a transition to a write enable input (column 9, lines 39-45).

Regarding claim 4, *Ahmad et al.* discloses using transition from HIGH to LOW logic levels (column 3, lines 1-15).

Regarding claims 5 and 6, *Malek-Khosravi et al.* discloses (Fig. 1; and column 2, line 66 to column 3, line 4) that the pulse width can be selected by the user with various inputs. At the time of the invention, it would have been obvious to incorporate into *Ahmad et al.* the teaching of *Malek-Khosravi et al.* for the purpose of parametrically varying the pulse width, and as desired.

Regarding claim 7, *Ahmad et al.* discloses that the configuration is fuse programmable (column 10, lines 25 ff).

Regarding claim 8, *Ahmad et al.* discloses that the configuration inputs are determined by a metal masking step during fabrication (column 3, lines 39-51).

Regarding claim 9, *Ahmad et al.* discloses that the technique can be used to test static random access memory (SRAM) cells (column 7, lines 44-48).

Regarding claim 10, *Ahmad et al.* discloses that the test circuit is configured to predict failure of one or more cells (Figs. 3-5; column 4, lines 23-32; and column 9, line 58 to column 10, line 10).

Regarding method claim 12, *Ahmad et al.* discloses a method of testing an integrated circuit (column 9, line 12) comprising the steps of: (A) entering a test mode (column 9, line 20); (B) measuring the operation of said integrated circuit (column 8, lines 3 ff) in response to a test signal generated (by the oscillator 55) on the integrated circuit (Fig. 2) in response to a control input 53); and (C) detecting failure of said operation (column 6, lines 33-41).

Ahmad et al. does not expressly disclose that the test signal has a predetermined pulse width and a method of predicting failure of the integrated circuit, prior to life testing.

Malek-Khosravi et al. discloses a method of testing an integrated circuit chip in which a variable pulse-width system is used to determine the minimum pulse width at which the system will operate properly (column 3, lines 17 ff).

Applicant's own admitted prior art (Fig. 1; and pages 1-2 of specification) discloses that there is a definite correlation between write end time (minimum pulse width for proper operation of the cell) and probability of failure.

Therefore, at the time of the invention, it would be obvious for a person of ordinary skill in the art to have combined into *Ahmad et al.* the teaching of *Malek-Khosravi et al.*, in light of the *Applicant's own admitted prior art* for the purpose of a method for predicting failure of an integrated circuit, so that circuits with a high probability of failure can be eliminated from further testing and/or can be repaired.

Regarding claims 13 and 14, *Ahmad et al.* discloses a write operation and a write pulse (column 9, lines 46 ff).

Regarding claim 15, *Ahmad et al.* discloses a pulse width determined by the data setup (oscillator 55).

Regarding claim 16, *Ahmad et al.* discloses life testing (abstract).

Regarding claim 17, *Ahmad et al.* discloses a sorting step following the testing (column 10, lines 23 ff).

Regarding claim 18, *Ahmad et al.* discloses repairing faulty integrated circuits (column 2, line 39).

Regarding claim 19, *Ahmad et al.* does not expressly disclose that the failure comprises a poor contact in cross-coupled latch transistors in a memory cell. The *Applicant's own admitted prior art* discloses that "SRAM cells fail due to poor contacts in cross-coupled latch transistors"

(specification, page 1, lines 17-18). Therefore it would have been obvious for a person of ordinary skill in the art to combine the teachings of *Applicant's own admitted prior art* into *Ahmad et al.*, and *Malek-Khosravi et al.*, for the purpose of identifying the cause of the failure of the integrated circuit, so that it can possibly be repaired.

Regarding claim 20, *Ahmad et al.* discloses, even within the context of well known prior art, voltage control of the tests (column 3, lines 1-15).

Regarding claims 21-23, *Malek-Khosravi et al.* discloses a plurality of pulse widths (abstract; and Fig. 2), a sequence of pulse widths (Fig. 2; column 2, line 63; and column 3, lines 9-11) and different circuits for generating them (Figs. 1-6). At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine into *Ahmad et al.*, the teachings of *Malek-Khosravi et al.*, in light of the *Applicant's own admitted prior art*, for the purpose of having versatile control over the pulse-width inputs.

Discussion of Applicants' Arguments

9. Applicants' arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection. However, since some of the arguments are concerned with *Ahmad et al.* which is also used in the present rejections, the Applicants' arguments on *Ahmad et al.* are considered below.

The Applicants argue that (beginning at the bottom of page 15 of response): "Ahmad does not disclose or suggest a **test circuit configured to generate a test signal having a**

predetermined pulse width in response to a control input... " (emphasis in original). In this argument, the Applicants argue against the references individually. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). *Malek-Khosravi et al.* does disclose different pulse widths.

Also, the foregoing argument is unpersuasive in itself. In *Ahmad et al.* the test is initiated by the oscillator 55, on the chip. This oscillator does generate a pulse of "predetermined pulse width in response to a control input."

The Applicants also argue (Page 16 of response): "Ahmad **does not generate** the test enable signal..." (emphasis in original). Here the Applicants are arguing features not recited in the claims. Specifically, claim 1 only recites a "test signal," not a test enable signal.

Conclusion

8. Any inquiry concerning this communication should be directed to Dr. T. R. (Joe) Sundaram at telephone number (703) 308-6821. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, N. Le can be reached at (703) 308-0750.

T. R. Sundaram

January 14, 2003

N. Le
Supervisory Patent Examiner
Technology Center 2800